NetFPGA-PLUS: the next generation of NetFPGA platforms

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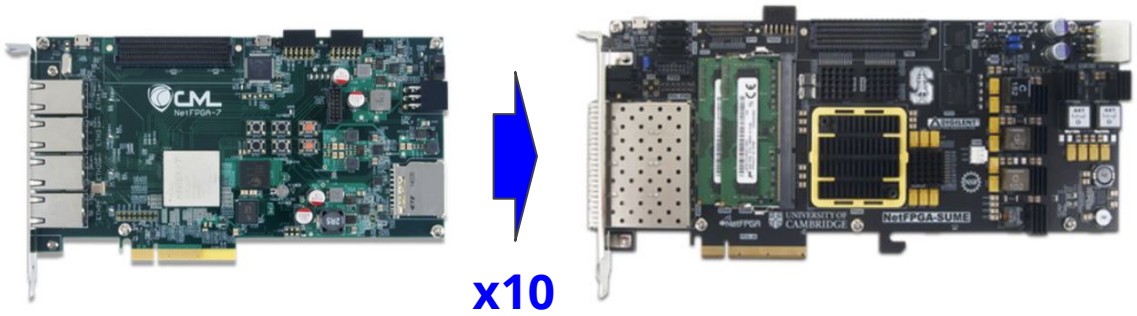
NetFPGA

NetFPGA is an open-source platform for line-rate prototyping of network devices (Switch, NIC, Router), used for research and teaching.



NetFPGA-CML (1GbE x4) NetFPGA-SUME (10GbE x4)

[Screenshot from https://store.digilentinc.com/ and https://www.xilinx.com/products/boards-and-kits/alveo/u250.html]

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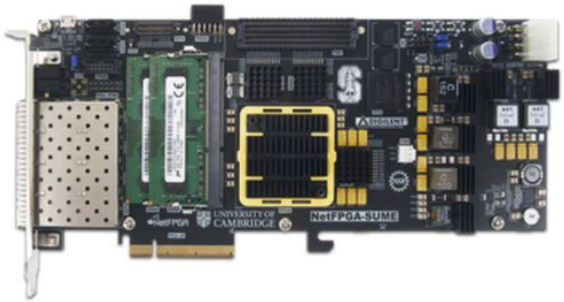
x10



x10

NetFPGA-CML (1GbE x4)

NetFPGA-SUME (10GbE x4)

NetFPGA-PLUS
on Xilinx Alveo(100GbE x2)

[Screenshot from https://store.digilentinc.com/ and https://www.xilinx.com/products/boards-and-kits/alveo/u250.html]

What is NetFPGA ?

- NetFPGA = Networked FPGA
- The FIRST Smart NIC
- Open source https://github.com/NetFPGA
- Successful projects, e.g.
  - Software Defined Networking - yes the entire industry!
    - Original Openflow device and specification prototype
    - Active target in P4 community
    - OFLOPS compliance tester
  - Network Datacenter Protocol
  - OSNT (Network Tester)

NetFPGA-PLUS

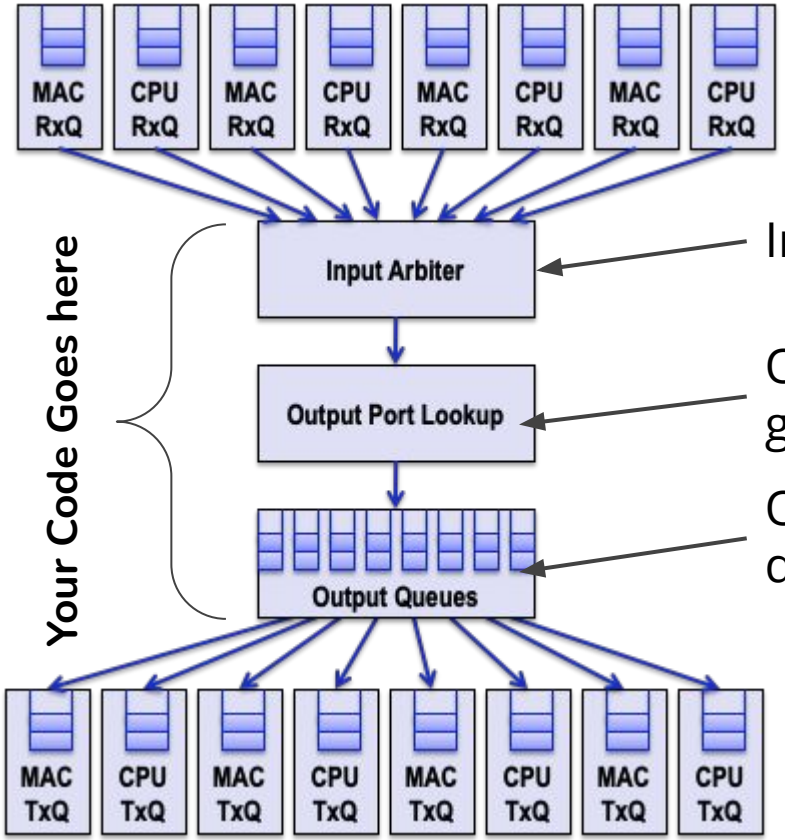
- Reference Projects - since the 1GbE platform
  - Learning switch
  - IPv4 Router
  - Network Interface Card (NIC)
- NetFPGA library modules
- Toolset for verification
  - Python scripts/library common codebase for
    - Program simulation and hardware verification
- Community: documentation, workshops, tutorials, etc.
- Xilinx Alveo board - so commodity support

All known benefits, on a new platform

Target Boards

- Alveo Series FPGA
  - Commercial Xilinx Products
    Alveo U200 /U250 / U280
  - Xilinx VCU1525 Eval board
- Platform features
  - Ultrascale+ FPGA
  - PCIe Gen3 x16
  - QSFP28 (100GbE) x2
  - DDR4 SDRAM 32GB/64GB
    HBM2 8GB (U280)

NetFPGA Pipeline - A common environment

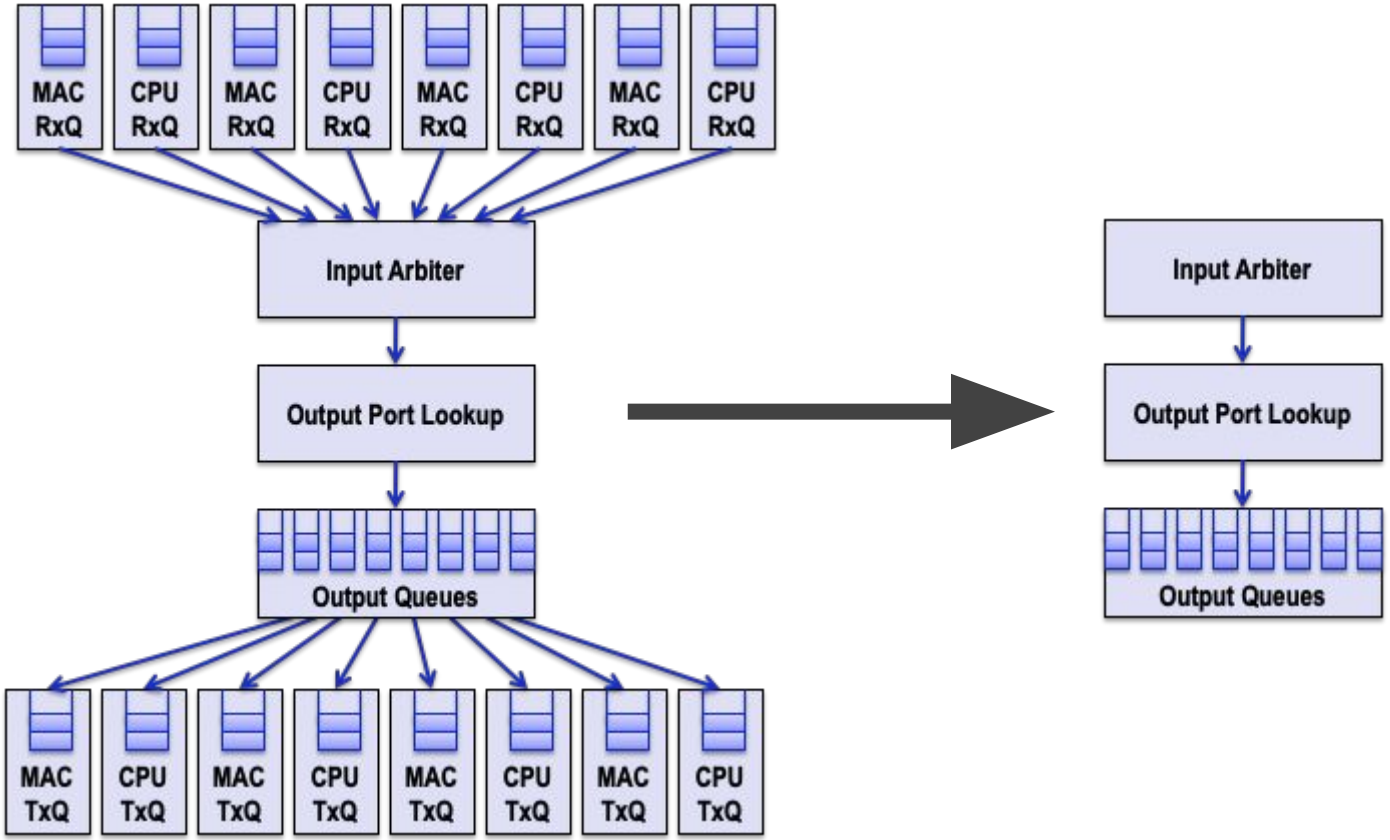


Input Arbiter - this is for your packet schedulers

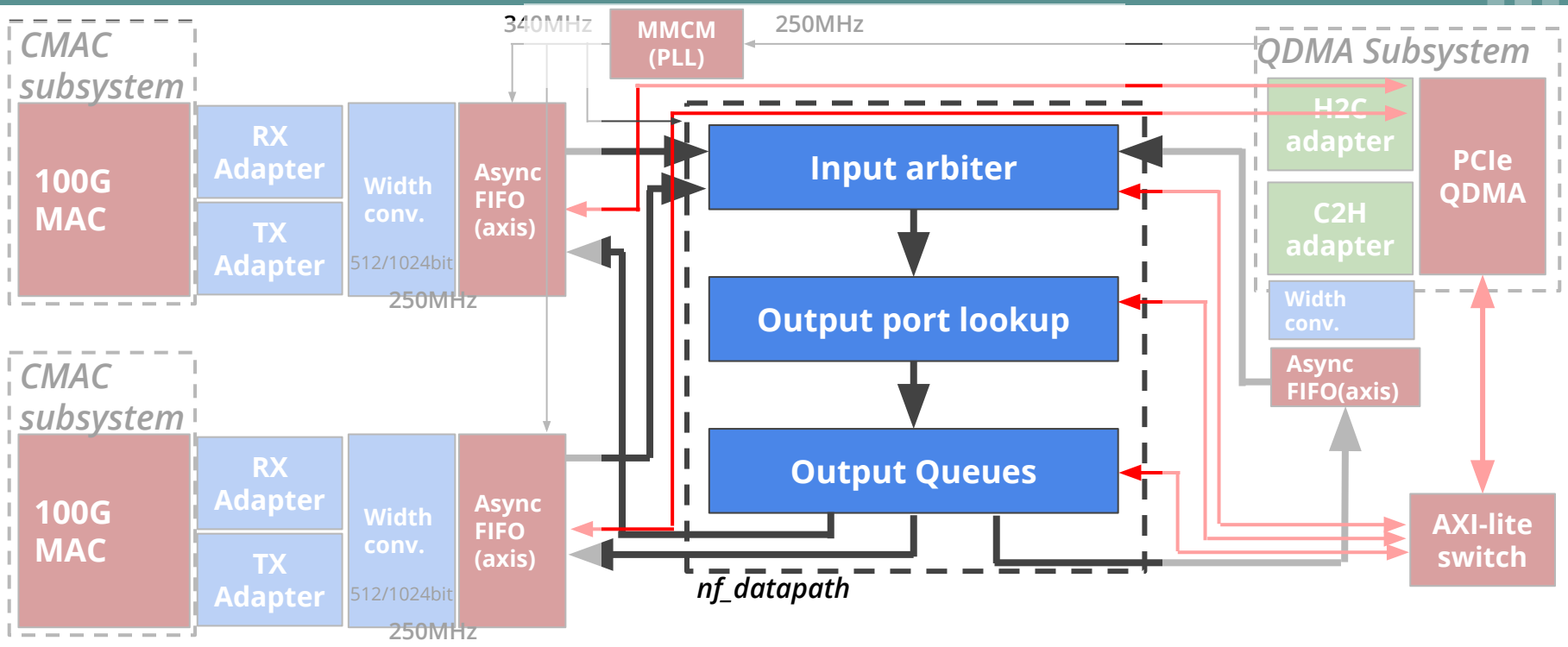
Output Port Lookup - Where should this packet go?

Output Queues - drop decisions and queue discipline

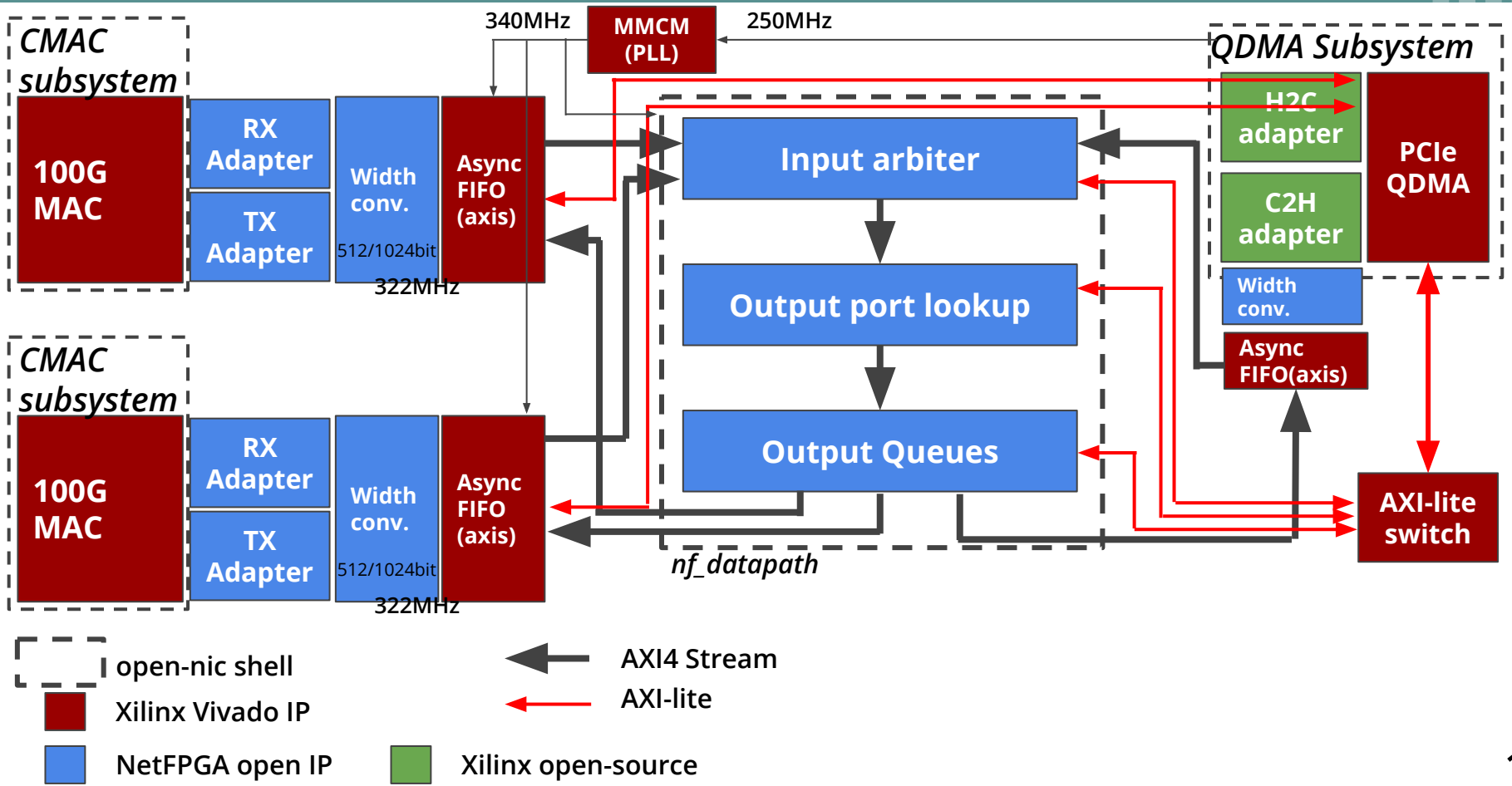
NetFPGA Pipeline - A familiar environment



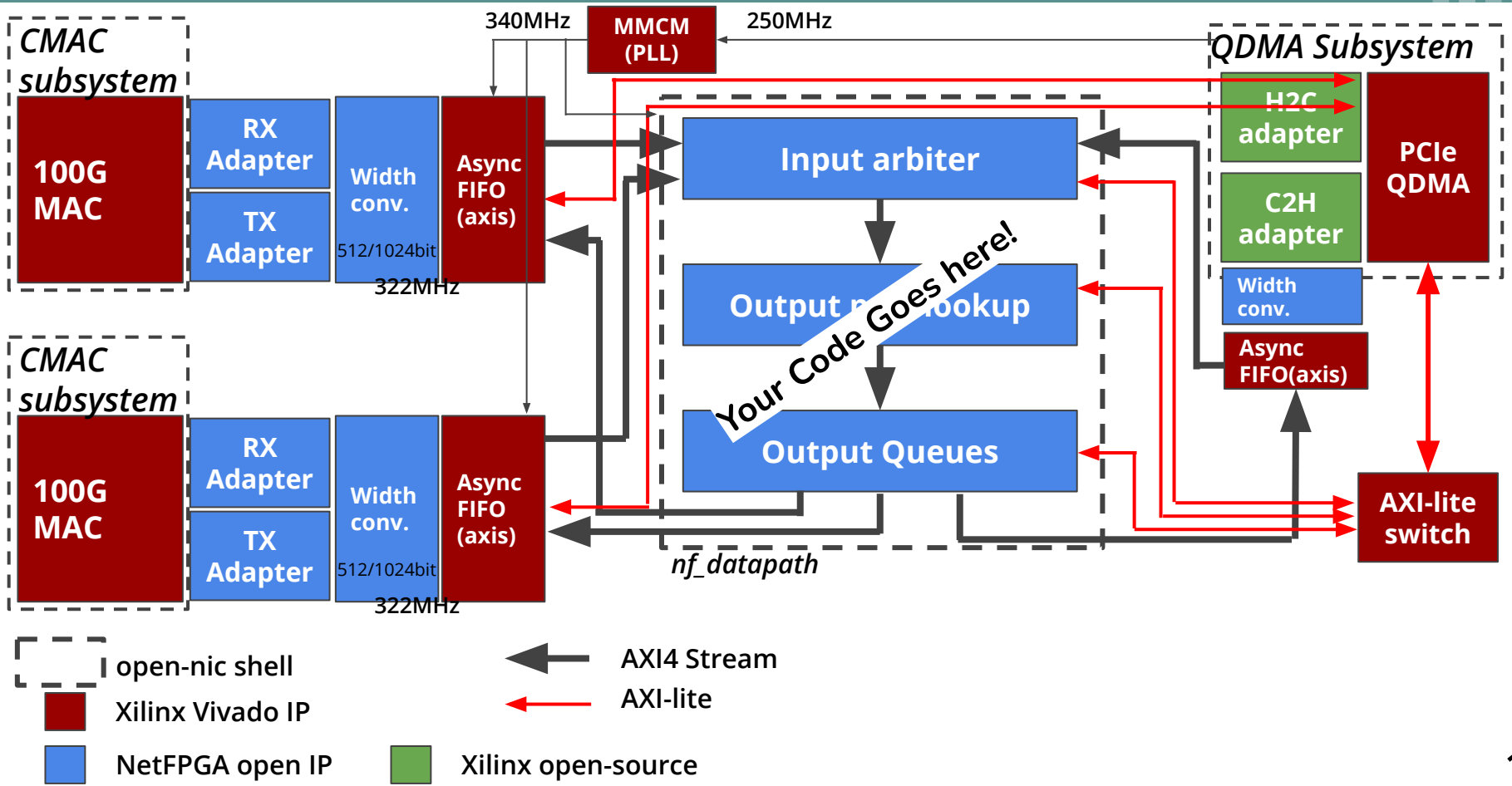
NetFPGA-Plus



NetFPGA-PLUS

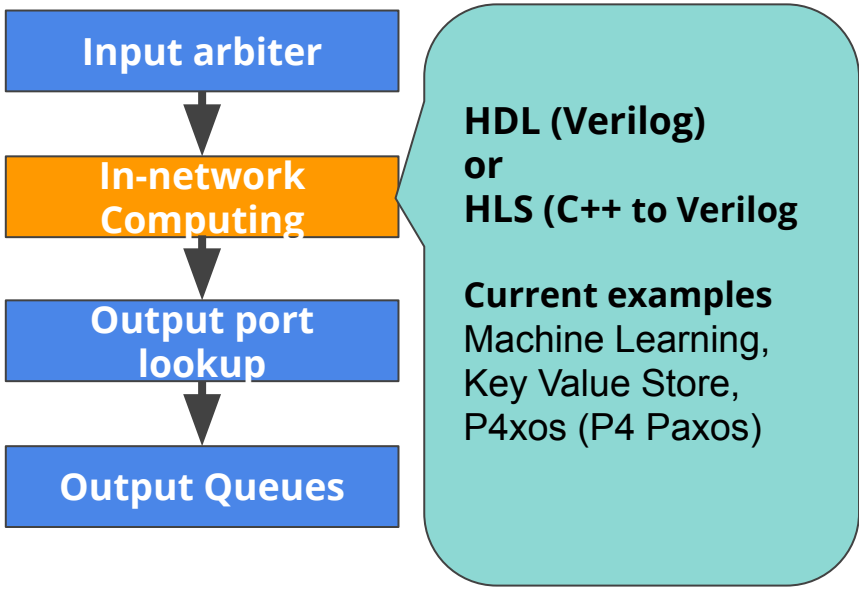


NetFPGA-PLUS



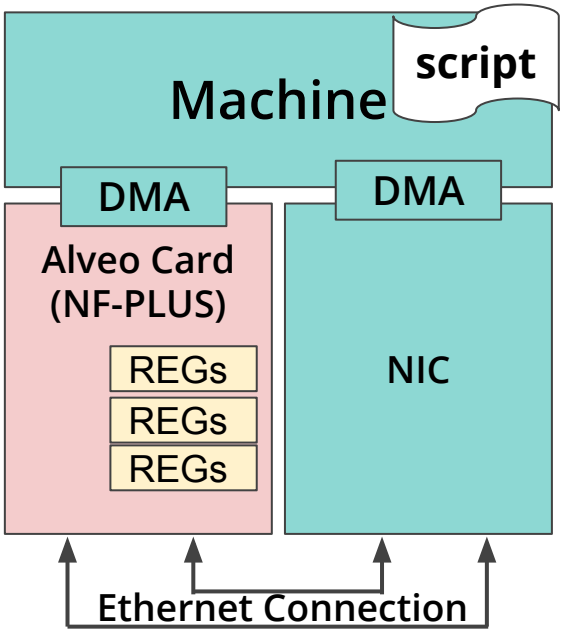
Develop your own application

- Even more SmartNICs
- In-network Computing
- Hardware Acceleration
- Network Measurement
- Network Functions
- Network Testing and Emulation



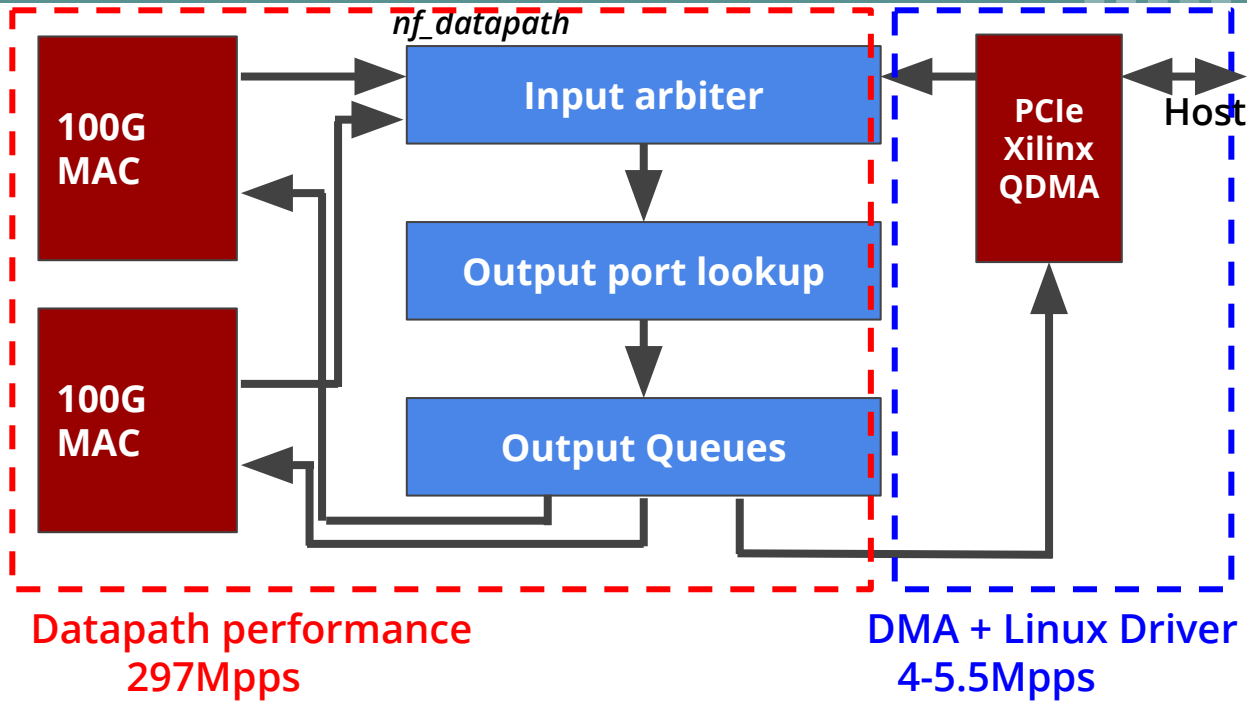
Verify your hardware and test it too

- python script for essential functions
  - Register checking
  - Pcap file comparison
- Keeping the environment familiar
  - Familiar scripts and library supporting
    - Code Simulation and Hardware Verification



Performance Note

- Learning Switch
  - **297M** pps datapath for 64B packets
- NIC (to/from host)
  - RX: **5.5M**pps for 64B
  - RX: **4M**pps for 1518B
- IPv4 Router
  - **34M** pps



2 x 100GE Full Line Rate at 64B!

Summary & Future work

- NetFPGA-PLUS
  - Rapid prototyping of smart network devices
  - 2 ports 100GbE on Xilinx Alveo
  - Line rate data path for small packet sizes
  - Toolset for tests, simulation, development
- Available once Xilinx *get their ducks in a row*

Future support

- P4→NetFPGA (new compiler)
- External Memory (HBM, DDR4) packet buffer
- Transceiver support for 8 x 10/25GbE