

Open-Source Network Tester on NetFPGA-SUME Platform

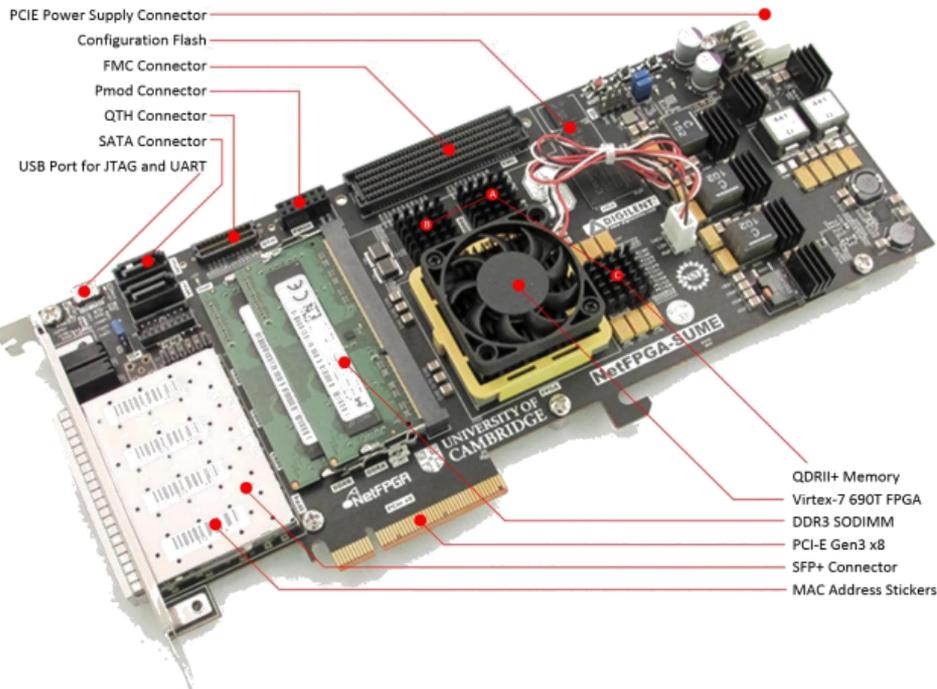
22nd June

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NetFPGA-SUME Specification

■ NetFPGA-SUME platform features



- Xilinx Virtex-7 XC7V690T FFG1761-3
- Two 4GB DDR3 SODIMMs 64 bit wide buses clocked at 850 MHz
- Three 72Mbit QDRII+ SRAMs 36 bit wide buses clocked at 500 MHz
- Two SATA III ports
- Micro-SD Card Slot
- Two 512Mbit flash modules
- PCI-E Gen3 x8 supporting 8Gbps/lane
- Four SFP+ interfaces supporting 10Gbps
- HPC FMC Connector

Open-Source Network Tester



- Collaboration project 2014 – Cambridge, Stanford, Princeton, CNRS, and Google.
 - Available on the NetFPGA-10G platform
 - NetFPGA-SUME port released Feb 2017 with new features
-
- Open source hardware and software platform for network test, publicly available
<https://osnt.org>
<https://github.com/NetFPGA/OSNT-Public/wiki>
 - Low cost, low jitter, flexible to update, scale-out, no CPU usage, nano-second resolution measurement

Commercial Network Testers

...this has led to a multi-billion dollar industry in network test equipment...

The logo for EXABLAZE features a blue square icon with a white double-headed arrow on the left, followed by the word "EXABLAZE" in a bold, blue, sans-serif font.The logo for EMULEX features a stylized, metallic-looking "E" symbol above the word "EMULEX" in a bold, black, sans-serif font.The logo for FLUKE networks features the word "FLUKE" in white, uppercase, sans-serif font above the word "networks" in a lowercase, orange, sans-serif font, all contained within a dark blue rectangular background.The logo for ixia features the word "ixia" in a bold, black, sans-serif font, with a red dot above the "i" and a blue dot above the "x".The logo for SPIRENT features a blue starburst icon above a blue curved line, with the word "SPIRENT" in a bold, blue, sans-serif font below.The logo for endace features an orange starburst icon above the word "endace" in a lowercase, grey, sans-serif font, with the tagline "power to see all" in a smaller, grey, sans-serif font below.

- Commonly closed and proprietary systems
- Limited flexibility
- Well outside the reach of most universities and research laboratories

Network Tester Comparison

- OSNT is flexible, high resolution, and full line rate performance at low cost

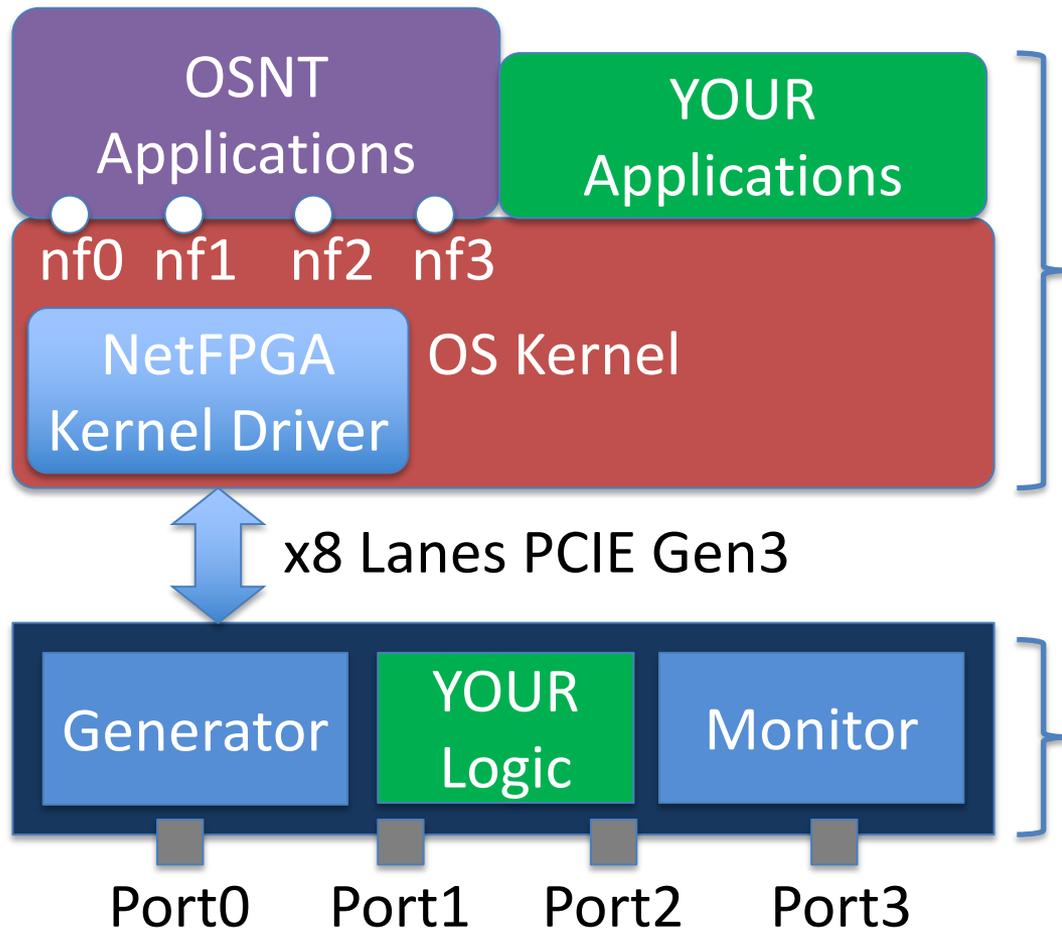
	Cost	Flexibility	Resolution	Line Rate
				
DPDK, SW tools				
				

OSNT-NetFPGA-SUME Main Features

- Open-Source Network Tester for HW packet traffic generation and monitor.
- Available on NetFPGA-10G and NetFPGA-SUME.
- 4x10Gbps traffic generation and monitor.
- High resolution timestamp at 6.4nsec (156.25MHz).
- GPS synchronized measurement system.
- QDR and DDR3 memory based traffic generator.
- Cut, Hash, and Batch processes to manage capture workload.
- HW and SW for the implementation are open-source.
- Flexible to modify and add more features...

OSNT System Configuration

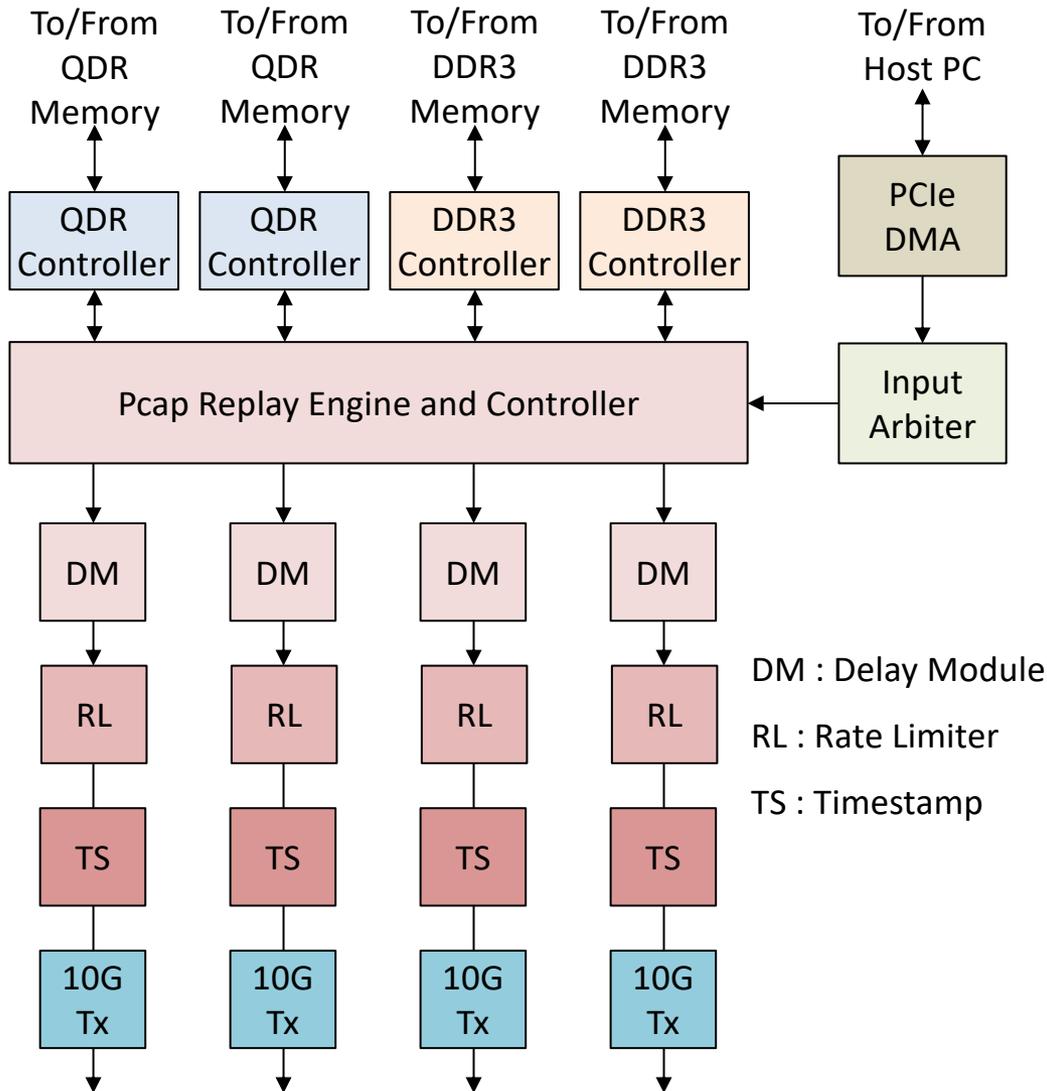
- Configuration of OSNT Systems on the NetFPGA-SUME platform



- Written in C, Python
- Open API and registers

- Written in Verilog HDL
- Users can add and modify the HW modules

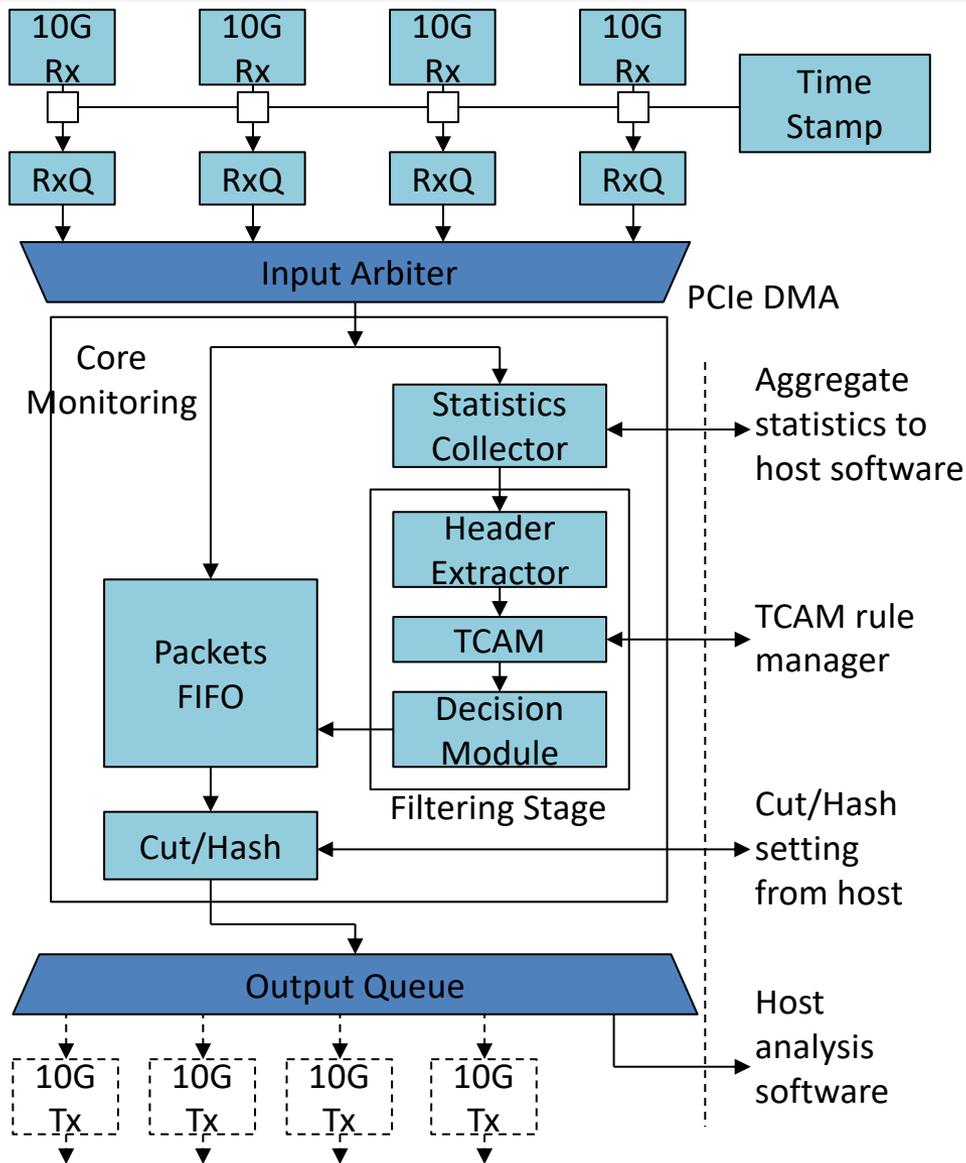
OSNT - Traffic Generator



Traffic generator FPGA HW structure

- 4x10G Pcap replay engine
- Pcap file controller
- Delay module
- Rate limiter
- Tx Timestamping

OSNT-Traffic Monitor



Traffic monitor FPGA HW structure

- Stats collector
- 4x10G packet capture
- TCAM-based Packet Filter
- Cut-Hash function

OSNT-Graphic User Interface

- OSNT GUI – Extensible Generator and Monitor GUI in Python.

Generator GUI

Console

PCAP ENGINE

Interface	Pcap File	Replay Cnt	Replay Cnt Display	Mem_addr_low	Mem_addr_high
0	1500.cap	100000000	100000000	0x0	0x30
1	Select Pcap File	0	0	0x30	0x30
2	Select Pcap File	0	0	0x30	0x30
3	Select Pcap File	0	0	0x30	0x30

RATE LIMITER

Interface	Rate Input	Rate Display	Enable	Reset
0	9.87Gbps	100.0000%	Enable	Reset
1	9.87Gbps	100.0000%	Enable	Reset
2	9.87Gbps	100.0000%	Enable	Reset
3	9.87Gbps	100.0000%	Enable	Reset

INTER PACKET DELAY

Interface	Delay Source	Delay Reg Input	Delay Reg Display	Enable	Reset
0	Set IPG	0	0ns	Enable	Reset
1	Set IPG	0	0ns	Enable	Reset
2	Set IPG	0	0ns	Enable	Reset
3	Set IPG	0	0ns	Enable	Reset

Timestamp Rx and Tx Position

Interface	RX TS Pos	TX TS Pos
0	0	0
1	0	0
2	0	0
3	0	0

Monitor GUI

Console

STATS

Port	Pkt Cnt	Vlan Cnt	IP Cnt	UDP Cnt	TCP Cnt	Pkts/s	Bits/s
0	12061355	0	12061355	12061355	0	822.368K	9.868G
1	0	0	0	0	0	0.0	0.0
2	0	0	0	0	0	0.0	0.0
3	0	0	0	0	0	0.0	0.0

FILTER RULES

Entry	SRC IP	SRC IP MASK	DST IP	DST IP MASK	L4 PORT	L4 PORT MASK	PROTO	PROTO MASK
0	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
4	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
6	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
7	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
9	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
10	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

CUTTER and TIMER

Cut to Length: N/A FPGA Timer: 183.13438784 Hash

OSNT-Command Line Interface

- Command-Line-Interface is also available to create a script automating the test process.

```
/root/osnt-sume-master/OSNT-SUME-live/projects/osnt/sw/host/app/tools
/root/osnt-sume-master/OSNT-SUME-live/projects/osnt/sw/host/app/tools 113x40
total 6256
drwxr-xr-x 2 root root 4096 Apr 11 13:31 .
drwxr-xr-x 7 root root 4096 Mar 25 10:53 ..
-rw-r--r-- 1 root root 2778 Apr 4 14:55 ext_mem_access.py
-rwxr-xr-x 1 root root 4624 Apr 11 13:30 gen_pcap_pkts.py
-rw-r--r-- 1 root root 0 Mar 25 10:53 _init_.py
-rw-r--r-- 1 root root 4749847 Apr 10 15:11 latency_dump_conv.pcap
-rw-r--r-- 1 root root 1512024 Apr 10 15:11 latency_dump.pcap
-rwxr-xr-x 1 root root 2772 Apr 10 14:48 osnt-test-template-1-2.sh
-rw-r--r-- 1 root root 2520 Apr 4 15:26 osnt-test-template-3.sh
-rw-r--r-- 1 root root 2696 Apr 4 15:25 osnt-test-template-5.sh
-rw-r--r-- 1 root root 2612 Apr 4 15:22 osnt-test-template-6.sh
-rwxr-xr-x 1 root root 2311 Mar 25 10:53 osnt-test-template-7.sh
-rw-r--r-- 1 root root 4 Apr 10 15:19 rd_reg32.dat
-rwxr-xr-x 1 root root 1665 Apr 11 13:31 run_pcap_gen.sh
-rw-r--r-- 1 root root 80364 Apr 10 15:11 tcpdump_latency_data.dat
-rw-r--r-- 1 root root 964 Apr 11 13:31 test_pcap_01.cap
-rw-r--r-- 1 root root 3192 Mar 25 10:53 timestamp_capture_cli.py
root@nf-test111:tools$
root@nf-test111:tools$
root@nf-test111:tools$ python ../cli/osnt-tool-cmd.py -ifp0 ../sample_traces/1500.cap -flt
0 10000 -rpn0 1000 -txs0 6 -rxs0 7 -lpn 1000 -lty0 -rnm
```

```
/root/osnt-sume-master/OSNT-SUME-live/projects/osnt/sw/host/app/cli
/root/osnt-sume-master/OSNT-SUME-live/projects/osnt/sw/host/app/cli 113x40
OSNT Monitor Stats (SUME-NetFPGA)
nf0 =>
Packet No : 0      Byte No : 0
VLAN No  : 0      IP No  : 0      UDP No : 0      TCP No : 0
=====
Pkt/Sec  :0.0      Byte/Sec :0.0

nf1 =>
Packet No : 0      Byte No : 0
VLAN No  : 0      IP No  : 0      UDP No : 0      TCP No : 0
=====
Pkt/Sec  :0.0      Byte/Sec :0.0

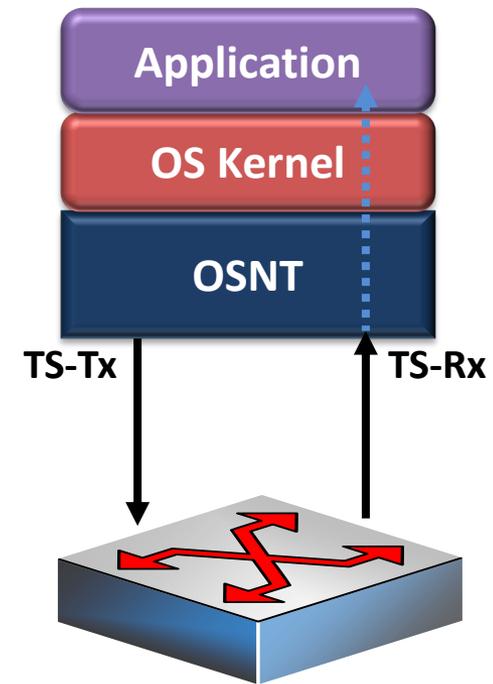
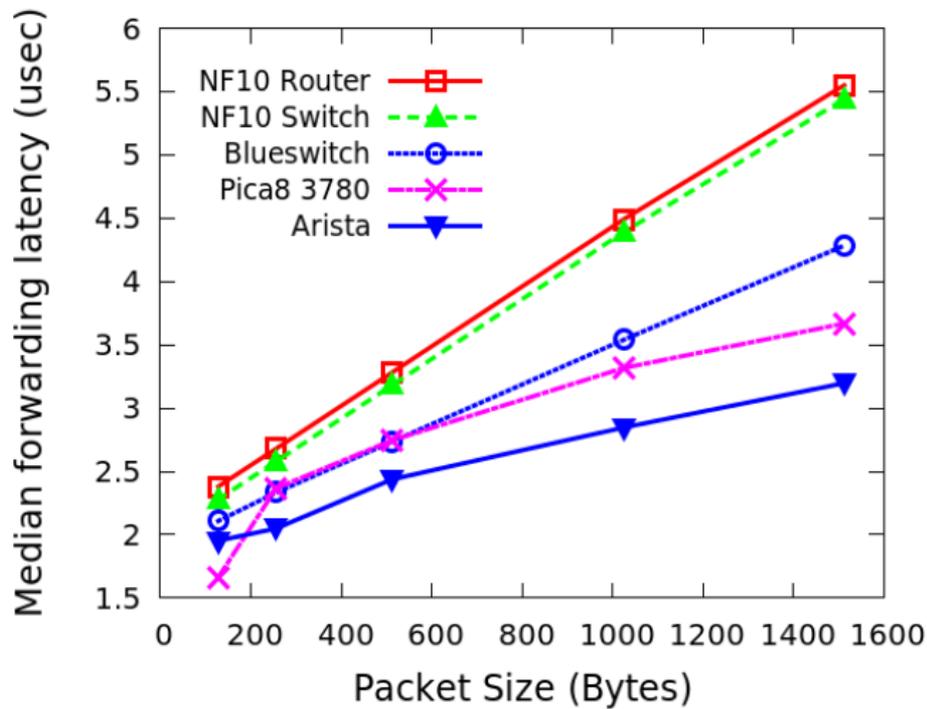
nf2 =>
Packet No : 0      Byte No : 0
VLAN No  : 0      IP No  : 0      UDP No : 0      TCP No : 0
=====
Pkt/Sec  :0.0      Byte/Sec :0.0

nf3 =>
Packet No : 0      Byte No : 0
VLAN No  : 0      IP No  : 0      UDP No : 0      TCP No : 0
=====
Pkt/Sec  :0.0      Byte/Sec :0.0

OSNT TimsStamp Counter: 34.381888 sec.  Cutter size : Disabled
Press Ctrl-C to exit...
```

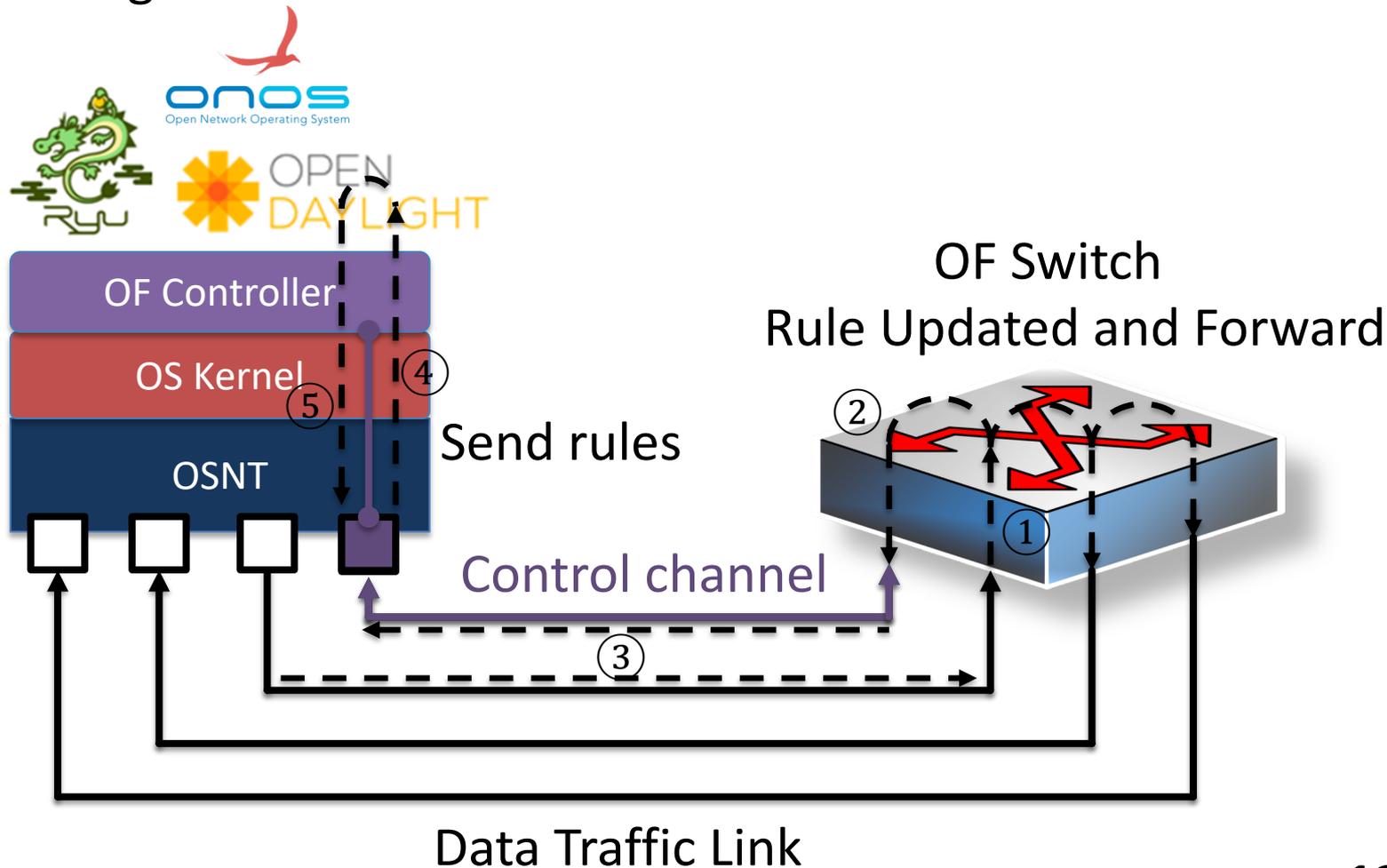
OSNT-Switch Latency Measurement

- Switch latency measurement results with OSNT against different packet lengths



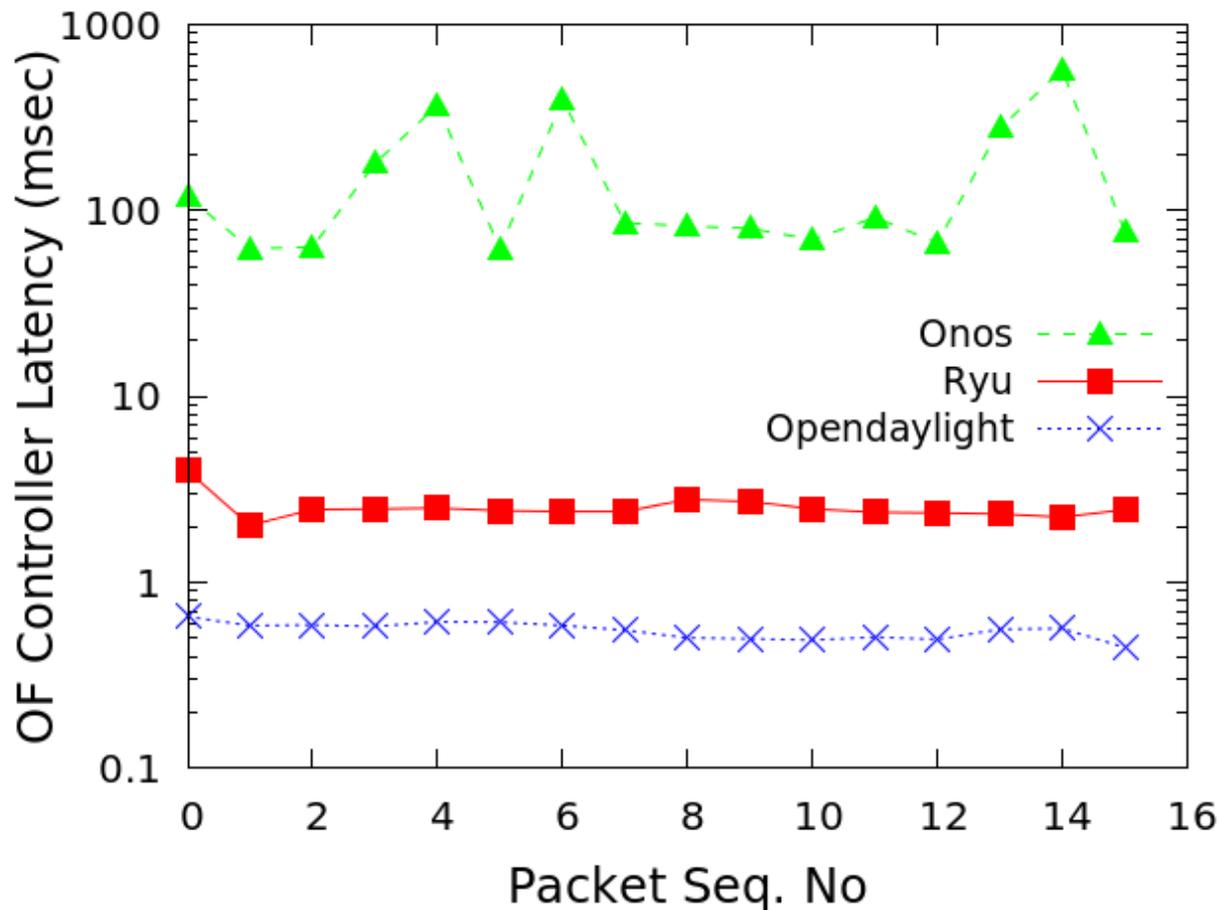
OSNT-OF Controller Latency

- Example Experimental Setup for Fine-Grain SDN measurement – L2 Learning Switch



OSNT-OF Controller Latency

- The latency results of the OF controllers measured by the OSNT – L2 Learning Switch latency between 4 → 5 by the controllers



OSNT-Reproduce Packet Traces

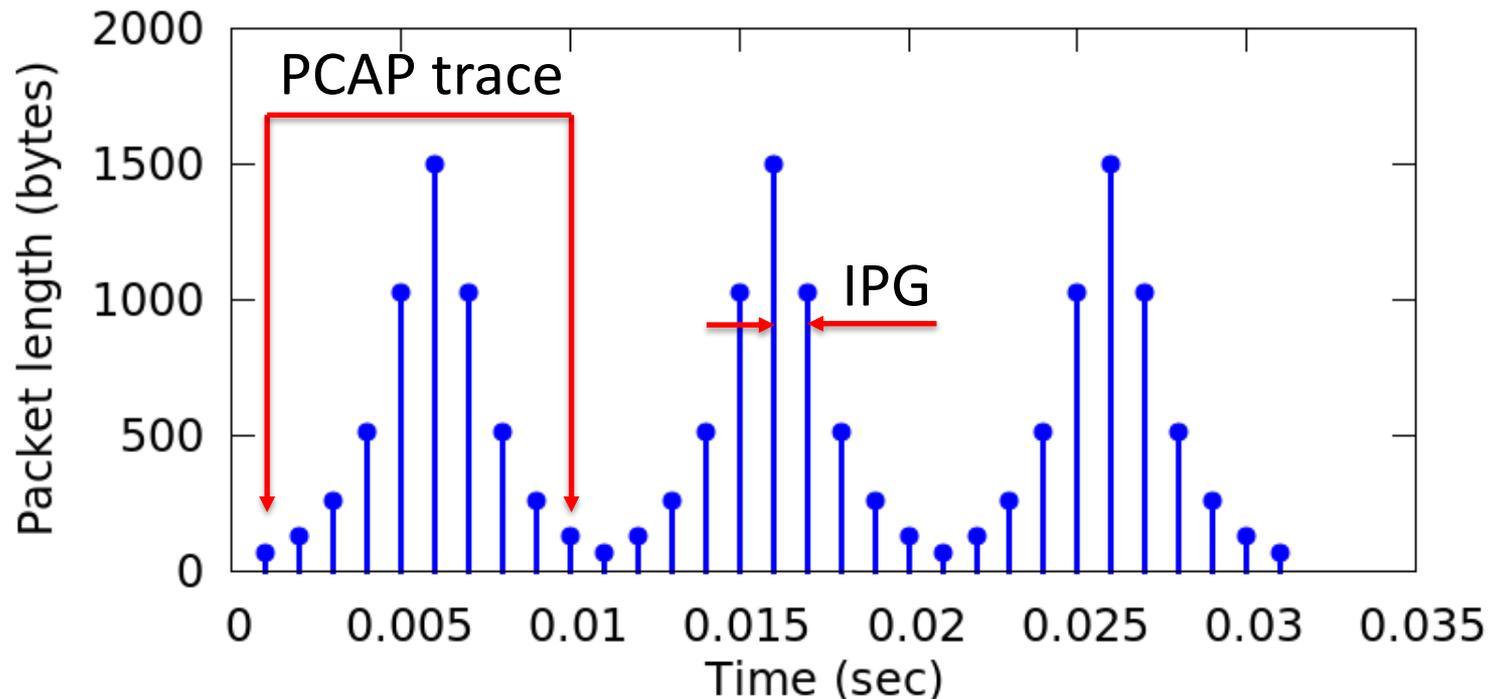
- Traffic generation with the timestamp in the PCAP traces
- Use created or dumped the PCAP traces with the timestamp
- Able to replicate and reproduce the same IPG traffic

Timestamp

```
01:00:00.100000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 22
01:00:00.200000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 86
01:00:00.300000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 214
01:00:00.400000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 470
01:00:00.500000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 982
01:00:00.600000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 1458
01:00:00.700000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 982
01:00:00.800000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 470
01:00:00.900000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 214
01:00:01.000000 IP 192.168.1.1.100 > 192.168.1.2.101: UDP, length 86
```

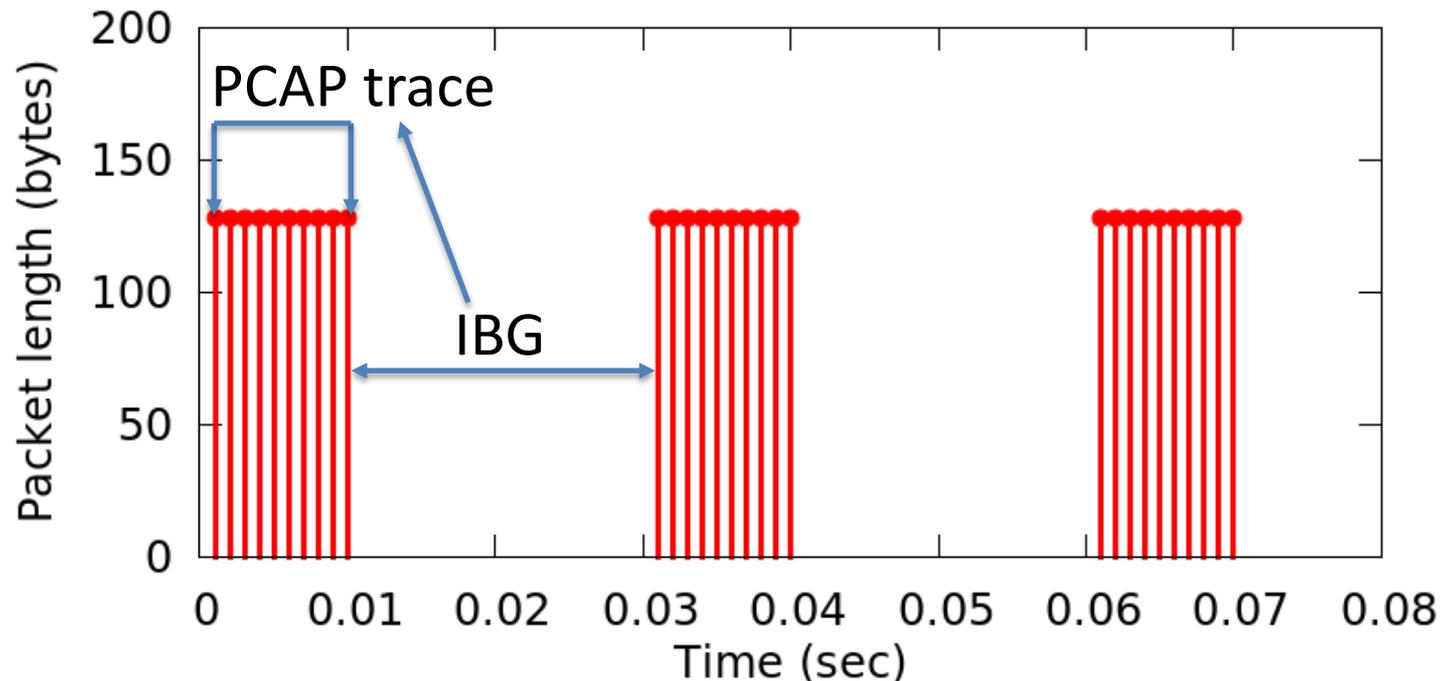
OSNT-Reproduce Packet Traces

- Traffic generation with the timestamp in the PCAP traces
- Use created or dumped PCAP traces with the timestamp
- Able to replicate and reproduce the same IPG traffic



OSNT-Reproduce Packet Traces

- Burst traffic generation with the timestamp in the PCAP traces
- Use created or dumped the PCAP traces with the timestamp
- Able to replicate and reproduce the same IPG and Inter-Burst-Gap (IBG) traffic



OSNT-SUME-live Github

- OSNT-SUME-live is publicly available.

NetFPGA / OSNT-SUME-live Private

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OSNT for NetFPGA-SUME board Edit

New Add topics

47 commits 1 branch 4 releases 3 contributors

Branch: master New pull request

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jhhan Merge branch 'master' of https://github.com/NetFPGA/OSNT-SUME-live Latest commit 1a058a2 7 days ago

contrib/challenge2017	NetFPGA design challenge 2017, added the first test	12 days ago
lib	Update the extmem packet replay controller and add the qdr i/f contro...	7 days ago
projects	Update minor in 10g rx and tx cores. Add comments to the timestamp mo...	a month ago
scripts	Add the first clean repo.	8 months ago
util	update pcap_gen to support configurable source and dest MAC addresses	12 days ago
Makefile	Add Makefile for ip core and sw driver generation.	
README.md	Update the release not link.	

README.md

OSNT

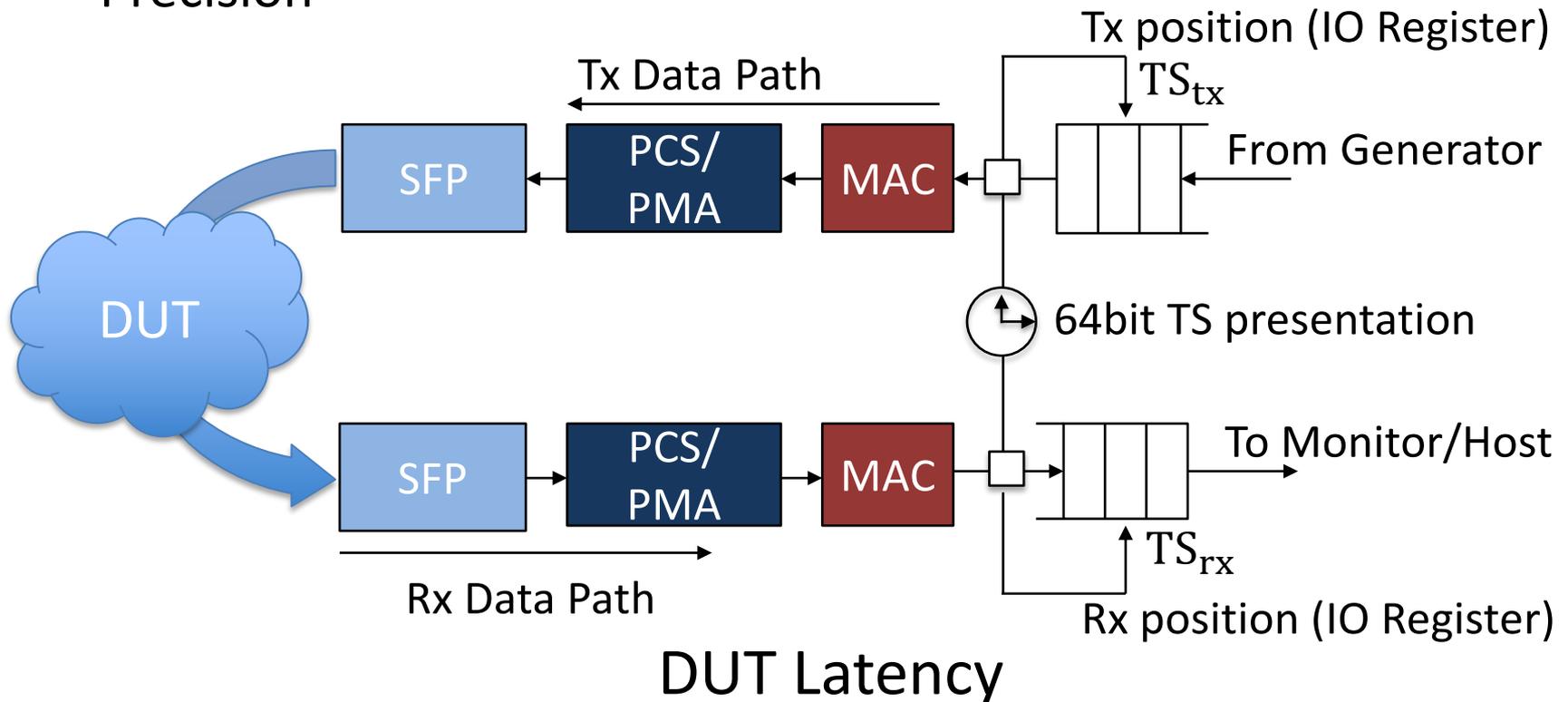


The image shows a NetFPGA-10G-SUMB board, a high-performance FPGA-based network interface card. It features a Xilinx Virtex-7 FPGA, a 10GbE SFP+ port, and various other components like memory, capacitors, and connectors. The board is labeled 'UNIVERSITY OF CAMBRIDGE NetFPGA-10G-SUMB'.

Q & A

OSNT-Latency Measurement

- Switch latency measurement with timestamp mechanism
- Timestamp - 64bit Fixed-Point representation with 32bit Precision



$$\Delta TS = TS_{rx} - TS_{tx}$$